TITLE: METHOD AND APPARATUS FOR REALIGNING BITS ON A PARALLEL BUS
INVENTOR(S) NAME: MATTHEW HAYCOCK ET AL.
DOCKET NO.: 884.455US1

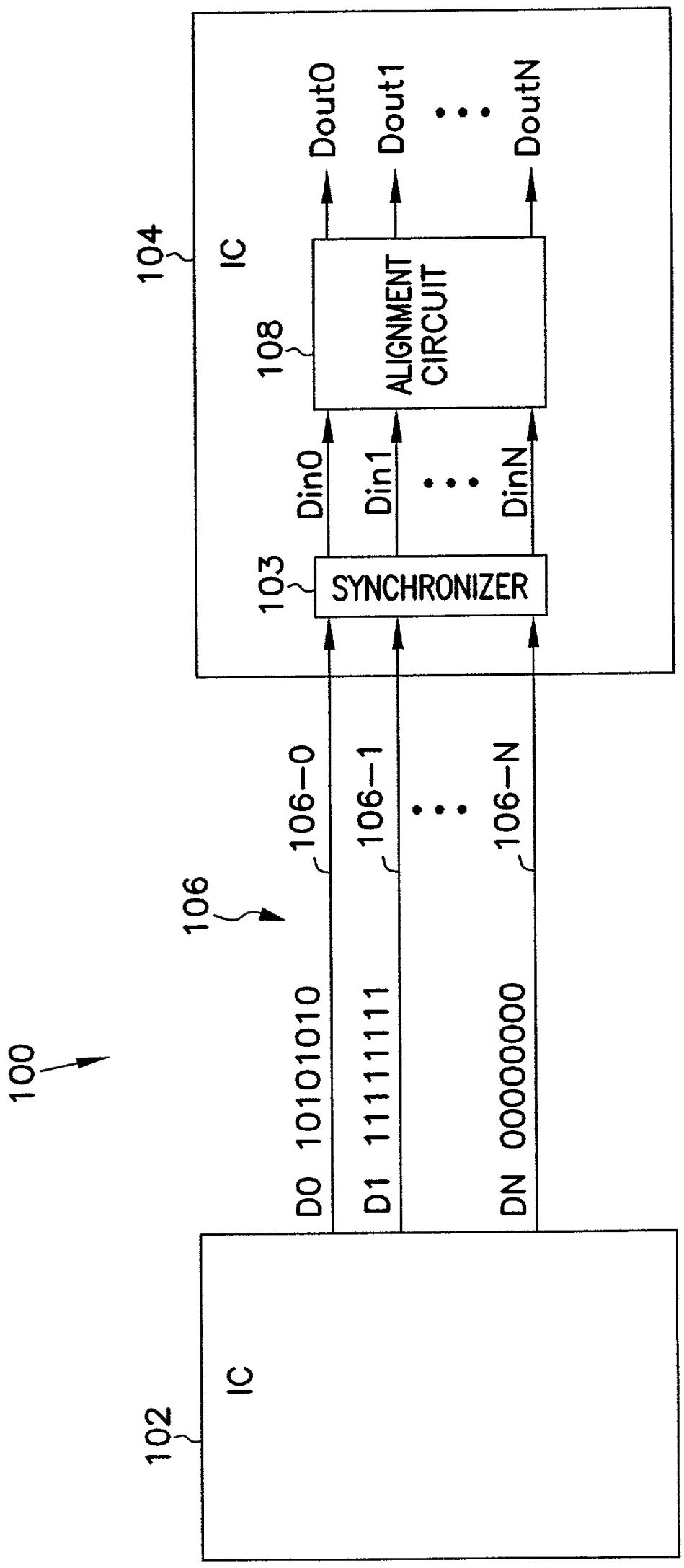

FIG. 1

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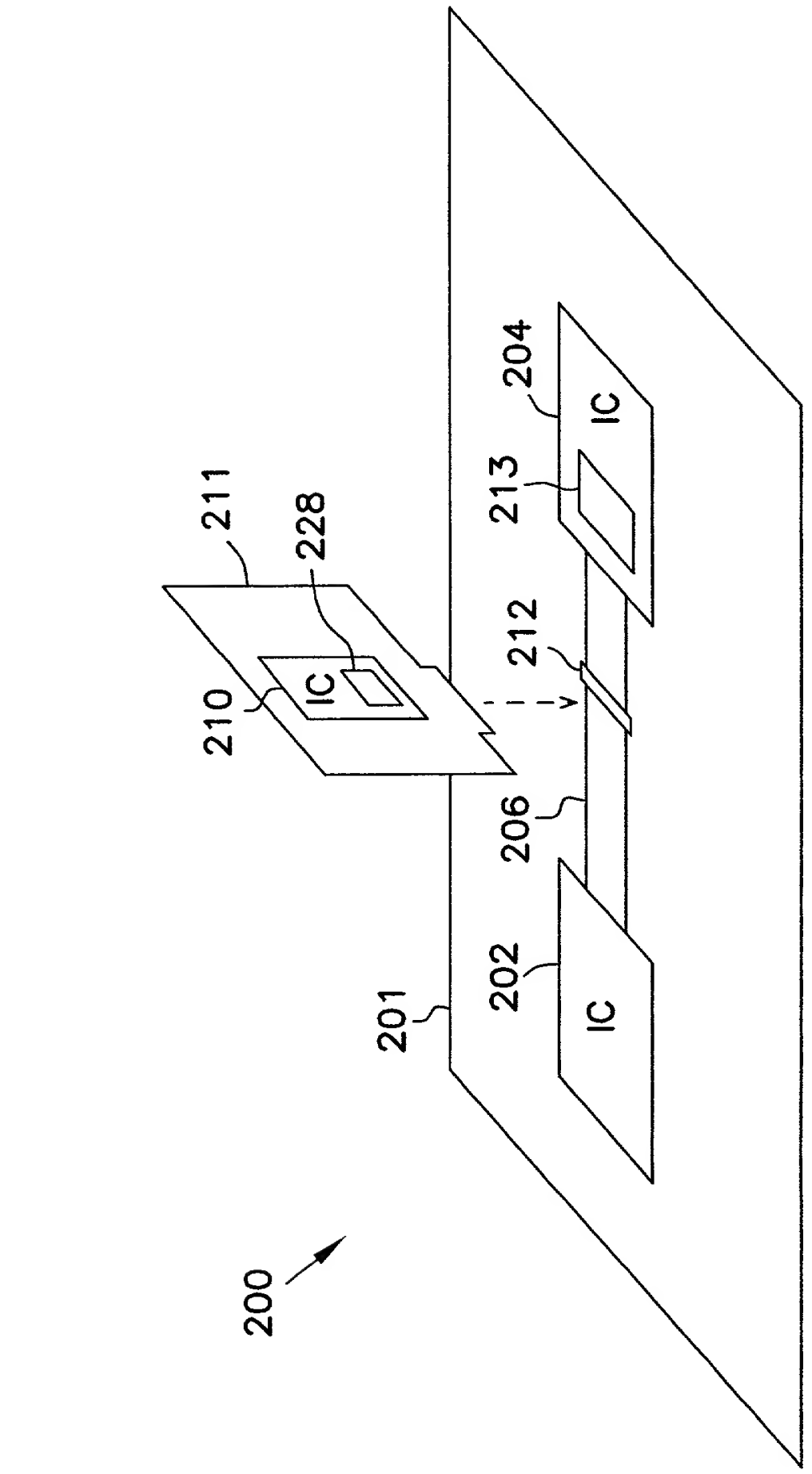

FIG. 2

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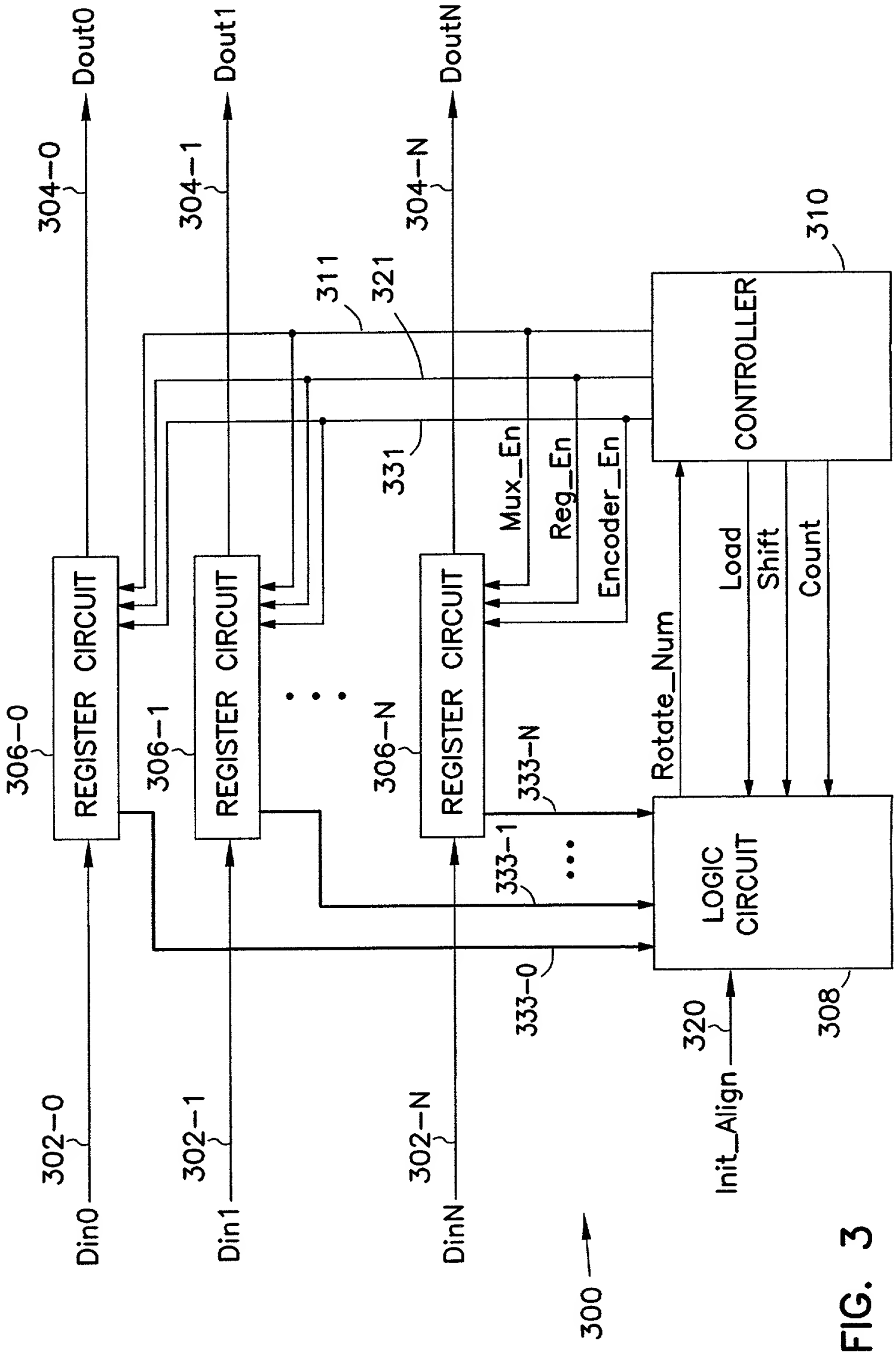

FIG. 3

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TRANSMITTED BITS:	1000010000	
DATA BIT #	RECEIVED AT 302 0–N	OUTPUT AT 304 0–N
0	1000010000	1000010000
1	0100001000	1000010000
⋮	⋮	⋯
N	0010000100	1000010000

FIG. 4

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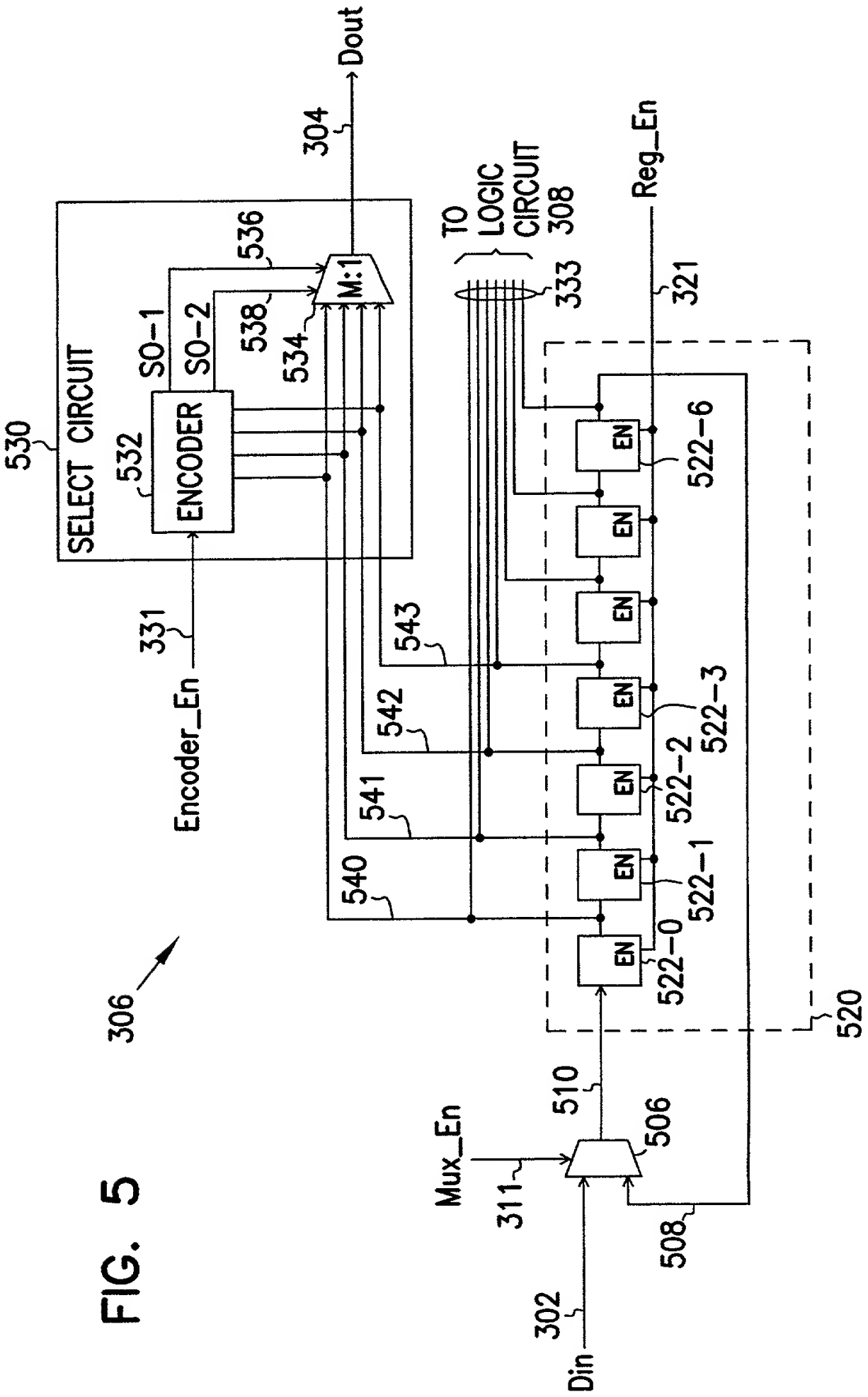

FIG. 5

TRAINING PATTERNS:	10000001000000100000...
RECEIVED PATTERNS:	
AT 1ST INPUT	10000001000000100000...
AT 2ND INPUT	01000000100000010000...
AT 3RD INPUT	00100000010000001000...
AT 4TH INPUT	10000001000000100000...

I1 I2 I3

FIG. 6

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CONTENTS OF:	7 BIT TIME INTERVALS
REGISTER 700	1000000
REGISTER 701	0100000
REGISTER 702	0000001
REGISTER 703	1000000

FIG. 7A

CONTENTS OF:	3 BIT TIME INTERVALS
REGISTER 700	0100000
REGISTER 701	0010000
REGISTER 702	1000000
REGISTER 703	0100000

FIG. 7B

FIG. 8A

CONTENTS OF:	COLUMN 0 ↓ ... COLUMN 6 ↓	
REGISTER 800	1000000	
REGISTER 801	0100000	
REGISTER 802	0000001	
REGISTER 803	1000000	
BIT–WISE OR	1100001	(RESULTANT LOGIC VECTOR)

FIG. 8B

	ARRAY	
ROW 0	1100001	(RESULTANT LOGIC VECTOR)
ROW 1	1110000	
ROW 2	0111000	
ROW 3	0011100	
ROW 4	0001110	
ROW 5	0000111	
ROW 6	1000011	

FIG. 9A

	BEFORE ROTATION
REGISTER 700	1000000
REGISTER 701	0100000
REGISTER 702	0000001
REGISTER 703	1000000

FIG. 9B

	AFTER ONE ROTATION
REGISTER 700	0100000
REGISTER 701	0010000
REGISTER 702	1000000
REGISTER 703	0100000

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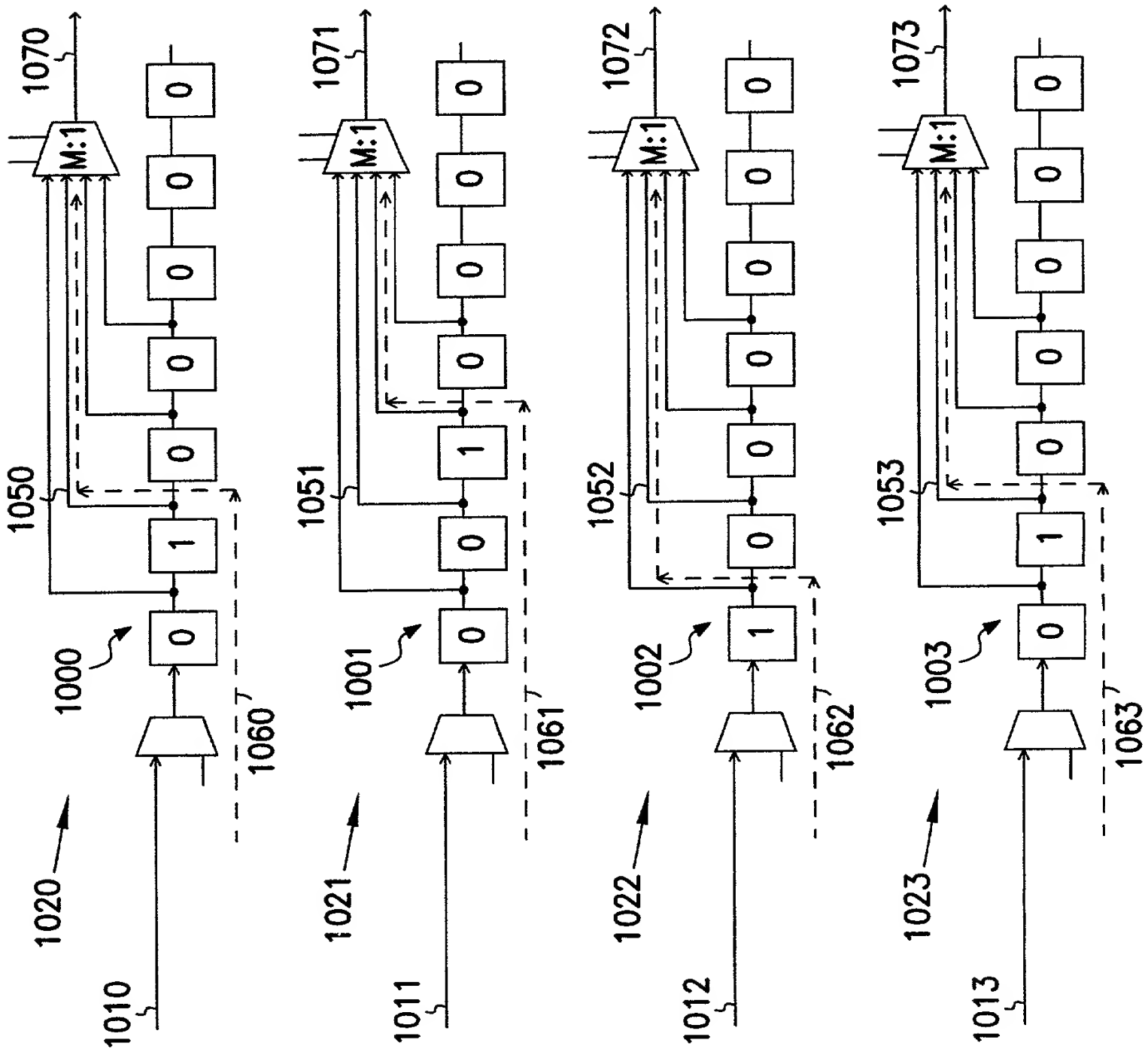
FIG. 10



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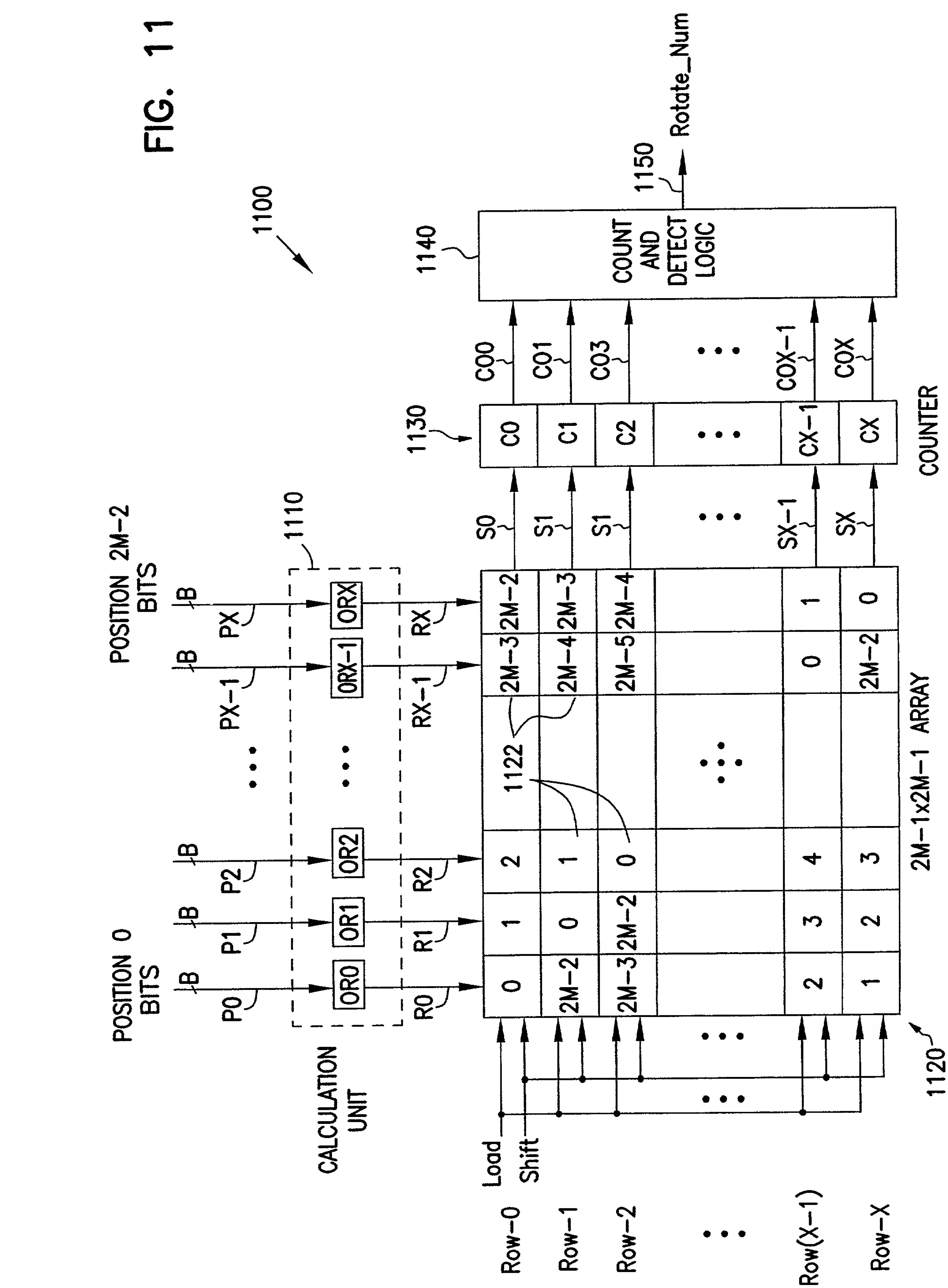

FIG. 11

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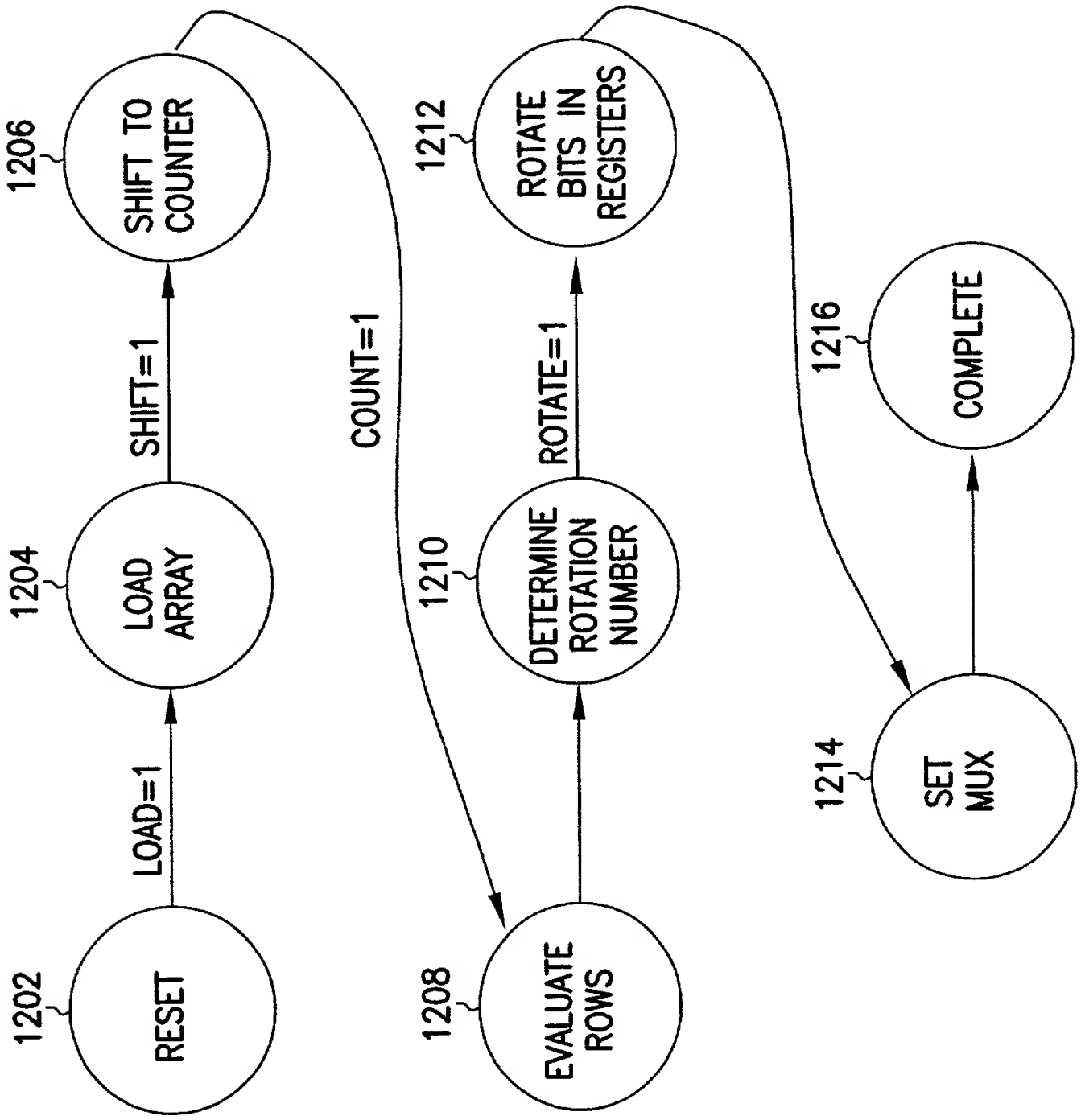

FIG. 12

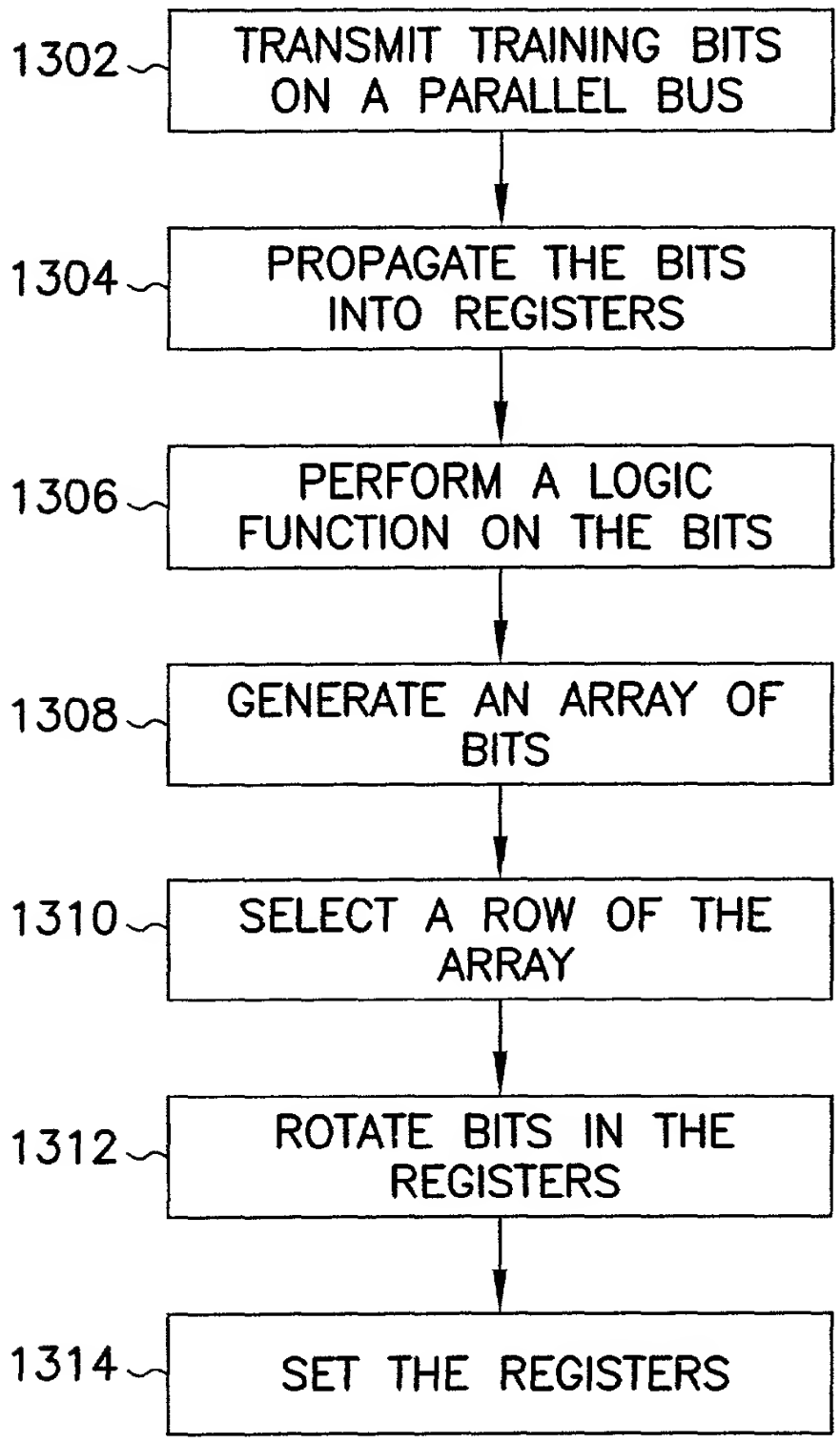
1302
TRANSMIT TRAINING BITS ON A PARALLEL BUS
1304
PROPAGATE THE BITS INTO REGISTERS
1306
PERFORM A LOGIC FUNCTION ON THE BITS
1308
GENERATE AN ARRAY OF BITS
1310
SELECT A ROW OF THE ARRAY
1312
ROTATE BITS IN THE REGISTERS
1314
SET THE REGISTERS

FIG. 13